PERFORMANCE CHARACTERISTICS OF INDUCTION MOTOR USING INVERTER TOPOLOGIES

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ABSTRACT

This paper presents the simulation and implementation of multilevel inverter fed induction motor drive. The output harmonic content is reduced by using multilevel inverter. In symmetrical circuit, the voltage and power increase with the increase in the number of levels of inverter. The switching angle for the pulse is selected in such way to reduce the harmonic distortion. This drive system has advantages like reduced total harmonic distortion and higher torque. The model of the multilevel inverter system is developed with PWM strategy to control the induction motor. The rate of change of voltage with respect to time i.e. dv/dt is very high at these edges, of the order of 500–5000 V/µs.The two-level inverter topology has attracted attention in low power low voltage drive applications where as Three-Level inverter topology has attracted attention in high power High performances voltage drive applications. Single-phase VSI cover low-range power applications and three-phase VSI cover the medium- to high-power applications. The Main purpose of these three level inverter topologies is to provide a three-phase voltage source, where the amplitude, phase, and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms Key words :Medium-voltage ac drives, multilevel converter topologies.

INTRODUCTION

Multilevel converters are considered for high-power medium-voltage drive applications, because the power structure can be realized with devices of lower voltage ratings [1]– [10]. A five-level inverter structure by cascading conventional two-level and three-level inverters is proposed in Part I of this paper [20]. An open-loop control scheme is presented in Part I to maintain dc-link capacitor voltage balancing and common-mode voltage (CMV) elimination in a dual five-level inverter-fed open-end winding induction motor (IM) drive, which effectively uses only the available redundant switching states of the inverter. It is pointed out that the proposed open loop controller is unable to take any corrective action to reduce the unbalance in the capacitor voltages that may arise.Every individual inverter is capable of generating three different voltage output +Vdc ,0, -Vdc by connecting the dc source to the ac output side by different combinations of the four switches S1 , S2 , S3 and S4 [1]. The synthesize ac output voltage waveform of the sum of all the individual inverter's outputs. The number of output phase voltage level of cascade multilevel inverter is 2s+1 where S is the number of dc sources. This outstandingly increases the level number of the output wave form and thereby dramatically reduced to the low order harmonics and total harmonic distortion. One of the foremost motives for developing the multilevel inverter is to reduce costSimilar voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters or by cascading a number of two-level inverters. However, the multilevel NPC inverters suffer from dc-bus imbalance, device underutilization problems and unequal ratings of the clamped diodes, etc., which are not very serious problems for inverters with three levels or lower. The capacitor voltage imbalance for a five-level one is presented in which suggest the need of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The cascaded H-bridge topology suffers from the drawbacks of the usage of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

PROPOSED CONVERTER TOPOLOGY

The proposed general configuration of "n" number of three level inverters connected in series is shown in Fig. 1. Each inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Fig. 1. If "Vdc" is the dc-bus voltage of each inverter module, then "α" is the turns ratio of each transformer and "n" is the number of inverter modules then for sine PWM (SPWM) strategy; the motor rms phase voltage (V_{Ph_motor}) can be expressed as follows Rms of $V_{ph\_motor} = \sqrt{3}\,\alpha m n V_{dc}/(2\sqrt{2})$ Where m is the modulation index of the inverter topology defined as follows $m = (\text{Peak of } V_{ph\_inverter})/(n\, V_{dc}/2)$ $V_{ph\_inverter}$ is the total phase voltage reference of the inverter topology. For the given peak of V_{Ph_motor}, peak of $V_{ph\_inverter}$ can be computed as follows Peak of $V_{ph\_inverter} = (\text{Peak of } V_{ph\_motor})/(\sqrt{3}\,\alpha)$ The generation of individual reference voltage signal of each inverter is discussed as follows. The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, "n" numbers of such three-level inverter modules require "2n" number of carriers [10], [13]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for R phase is shown in Fig. 2 for four series-connected three-level inverters. The carrier waves 1 and 1_ (Fig. 2) with R-phase voltage reference controls the inverter module 1. Similarly, 2 2_, 3–3_, and 4–4_ carrier waves with R-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously. Thus, the maximum dv/dt rate of the output voltage of this topology is limited to that of a single three-level inverter module.

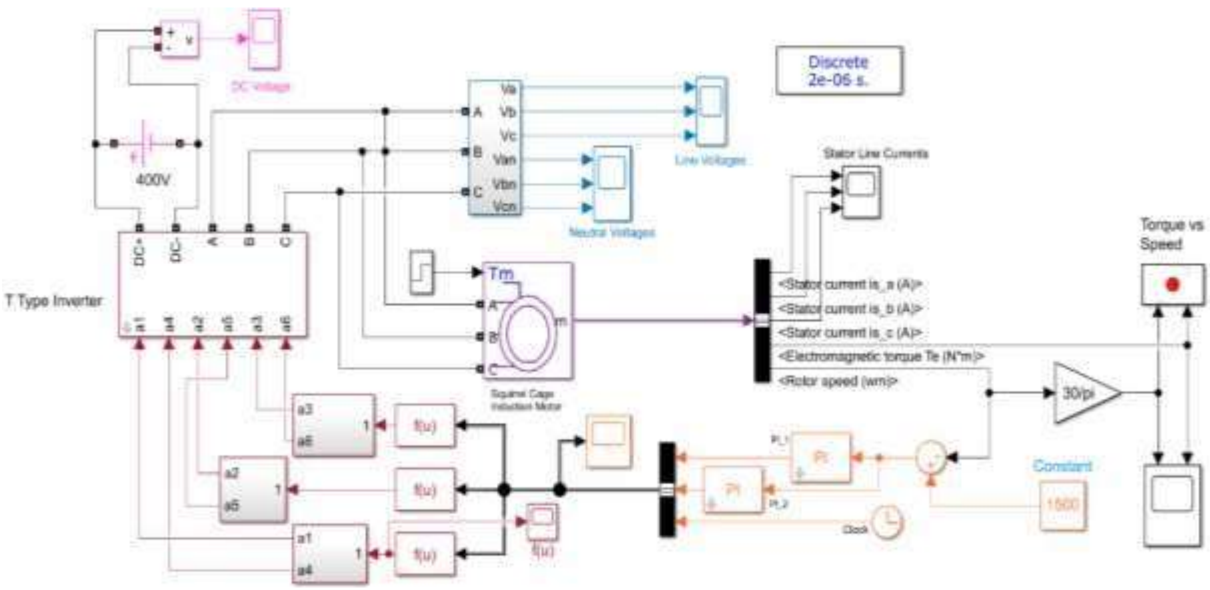
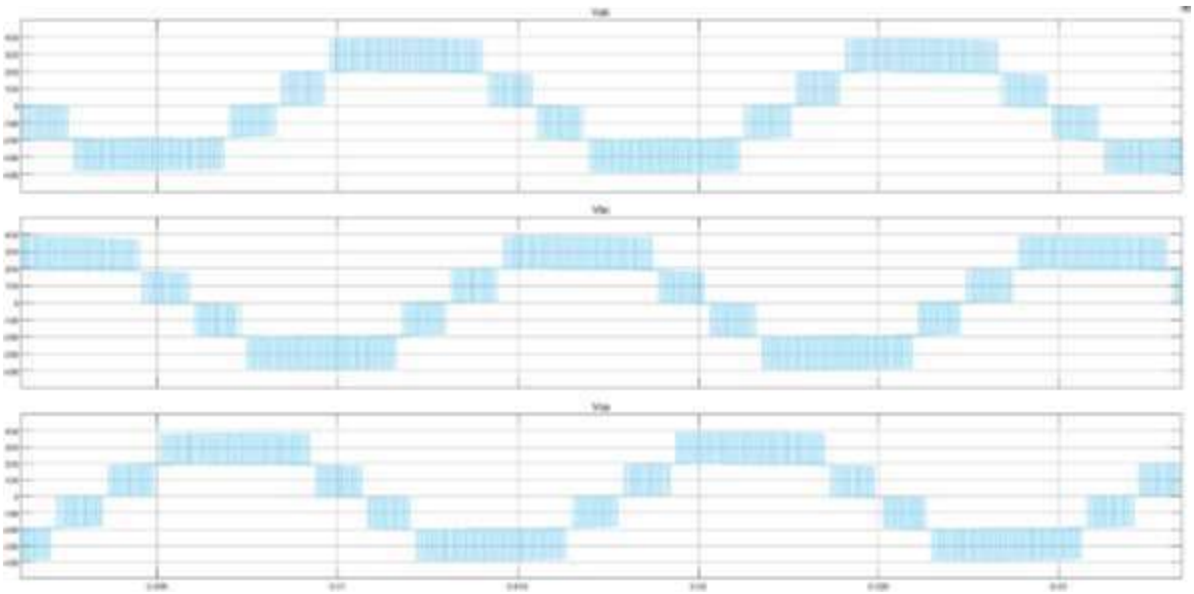


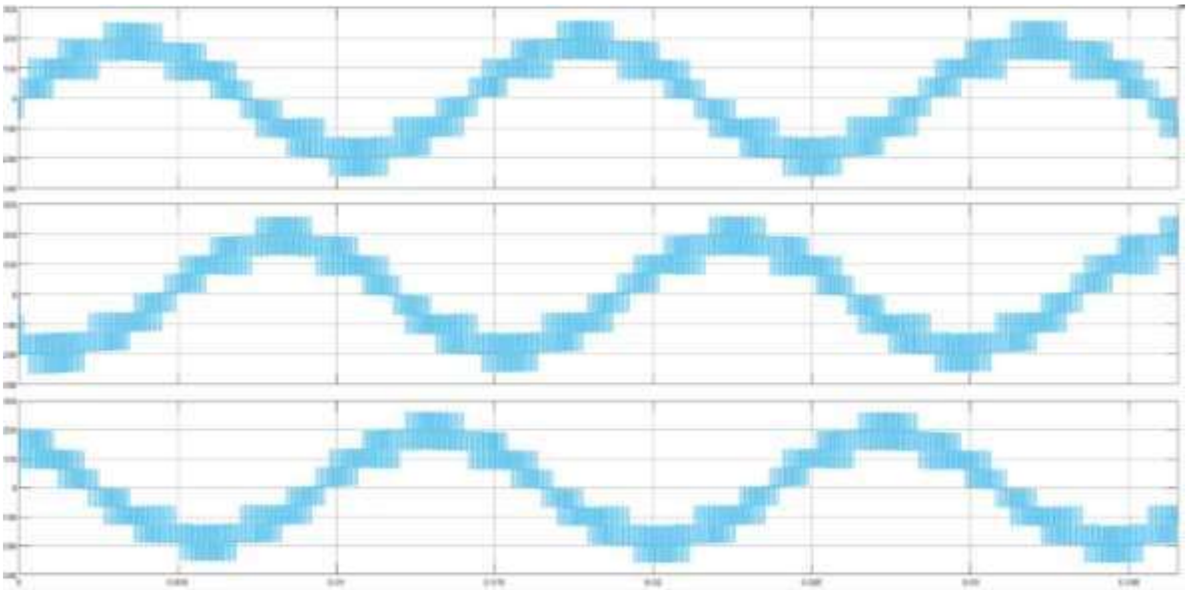
Fig 1 Proposed circuit configuration

TABLE-I (SWITCHING TABLE)

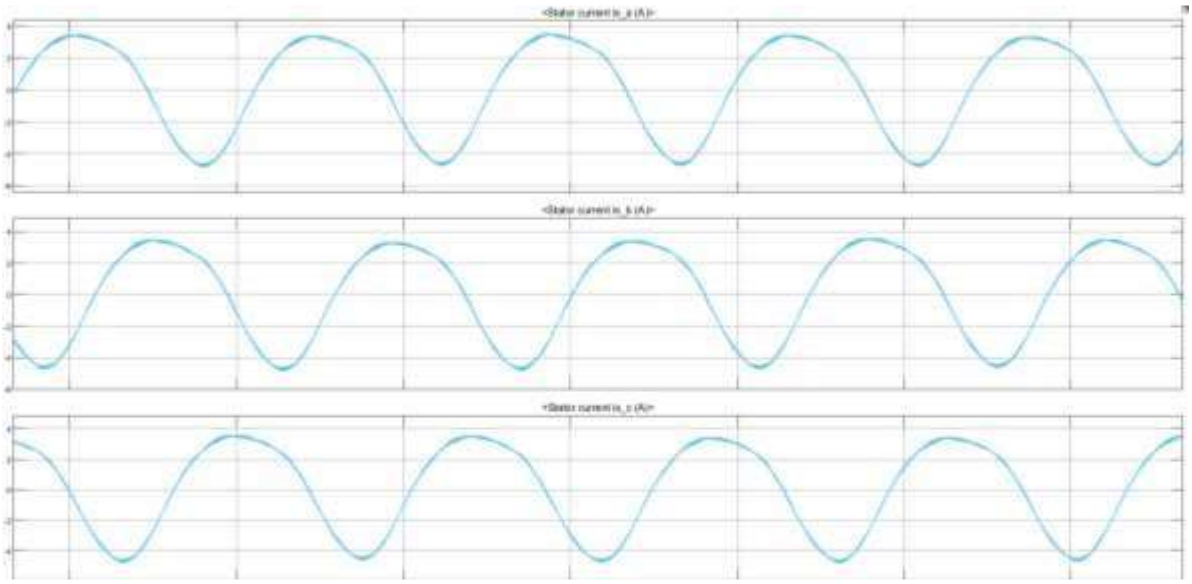
Generation of Level	Switching Devices				Output Voltage
	T1	T2	T3	T4	
+Vdc/2	on	off	On	off	+1v
0	off	on	On	off	0v
-Vdc/2	off	on	Off	on	-1v



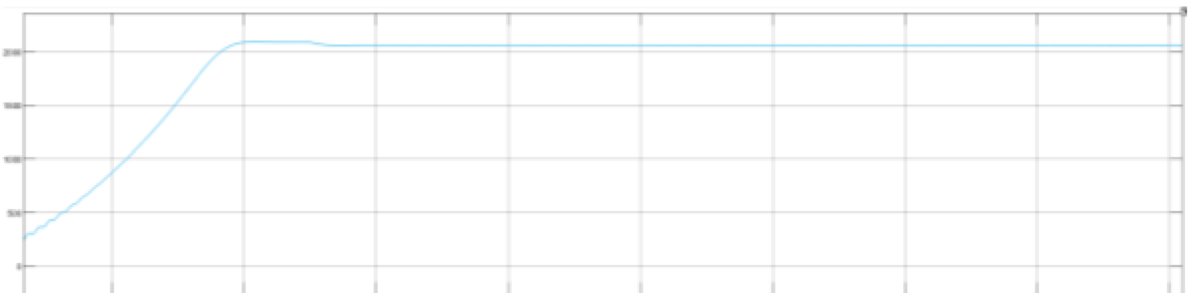
Neutral Voltages



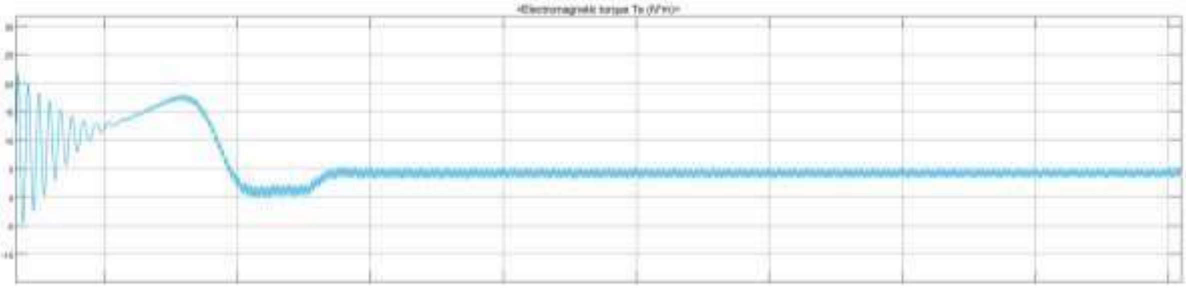
Stator Line Currents



Speed



Torque



No Load Torque vs Slip

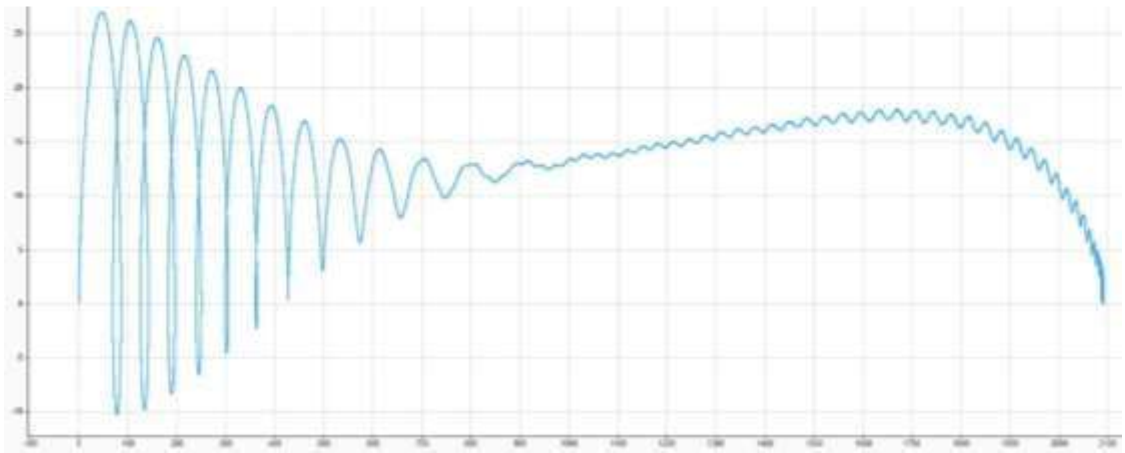


Figure (A)

CONCLUSION

A simulation model of systems consisting of a multilevel inverter and an induction machined has been developed a series connection of three-level inverters has been proposed for a medium-voltage SQIM drive with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc bus capacitor and reduced imbalance problems in the dc bus are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies. In this paper conventional and the cascaded multilevel inverter topologies were discussed and results were placed. Finally a Matlab/Simulink model is developed and simulation results are presented.

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